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GPS1005 DATA SHEET

GPS1005 – *A GPS RECEIVER FOR: EDUCATIONAL, ENGINEERING, SCIENTIFIC and R&D PURPOSES… COMPATIBLE WITH GPS OPENSOURCE CODE.*

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INTRODUCTION

This document contains data on the GPS Creations model GPS1005, PCI bus design, GPS receiver hardware. The GPS1005 is intended for the educational, engineering and scientific markets where experimental changes can be easily implemented. The GPS1005 consists of a PCI bus carrier card, it plugs into a PC where the OpenSource GPS object code resides. The majority of the GPS receiver hardware design is contained on the GPSRF board which is a smaller plug-in board installed on the PCI carrier card. The balance of the receiver's operation is accomplished within the PC.

FEATURES[1]:

- PC Based Solution, 100 MHz 486 Min Reqd.
- Runs OpenSource Code (C++)
- 12 Simultaneous Parallel Channels
- L1 Frequency Band, C/A Code
- GPSRF Board Consists of Zarlink GP2015 and 2021 Integrated Circuits
- Direct Interface to Correlators
- Only 1.25 Watts Consumed
- 5 Volts DC Feed for the GPS Antenna (Requires LNA gain of 26 dB minimum)
- Position Accuracy: 25 m 2dRMS without S/A
- 1 PPS output aligned within 500 nSec. (1 Sigma) of GPS

Accessories such as the GPS antenna or antenna kit are available through GPS Creations. Contact GPS Creations for more information on this and other GPS products. Request a copy of the "Product Guide".

Email: sales@gpscreations.com
for additional information.

[1]See GPS1005 Sales Brochure for specifications.

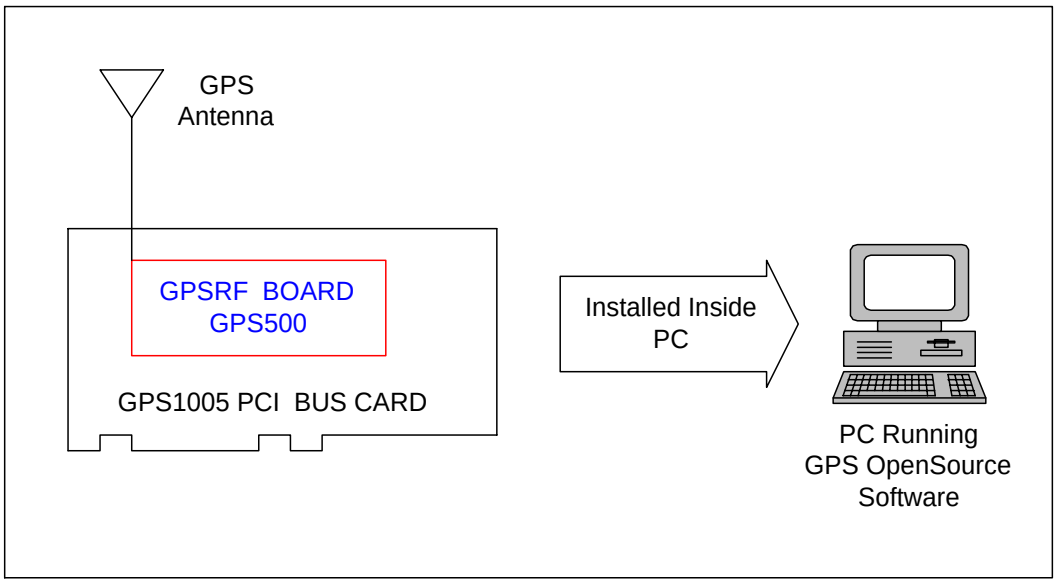

Figure 1 – GPS1005 Receiver System

GPS1005 RECEIVER DESCRIPTION

Section 1 - GPSRF Board

The GPSRF board is a modified version of an earlier GPS receiver design done by Plessey Semiconductor in the UK. Plessey, (now Zarlink Semiconductor) called their reference design the "ORION" board. It is one of the very few commercial GPS receiver designs broken down to this level of construction detail. Even the GPS receiver software is provided by Zarlink. However, it is only in object code format. The Orion design is fully described on the Zarlink website, for more detailed information, see: http://assets.zarlink.com/products/appnotes/an4808.pdf .

GPS Creations has taken the Orion design and used the Zarlink GP2015 and GP2021 IC's very much the same as Plessey did with their PCB layout. The difference being that the Orion design is a complete and stand-alone L1 band, C/A code, GPS receiver. The GPSRF board differs from the Orion board in as much as it interfaces with the various data, address and control lines of the GP2021 correlator IC and brings those lines out to a Personal Computer (PC) where the PC can be used to complete the GPS receivers' hardware and software tasks. The PC performs the functions of the microprocessor, memory (including disk storage of the GPS receiver OS), I/O interface, etc. The operational GPS software on the GPS1005 now runs on the PC instead of being burned into Read Only Memory (ROM) as it is on most conventional GPS receiver boards.

The GPSRF board can best be described as a RF "down-converter". The GPS satellites are transmitting at a frequency of 1575.42 MHz. The GPSRF board hardware receives those signals and down-converts them to "base-band" signals that can be processed by the PC. The GPSRF board is designed to work on a PCI bus PC card. The PCI card has electronic circuitry to couple the I/O lines to the PC and it uses a fixed I/O address of 304 to 30B (Hex). Future designs may use the GPSRF board with a USB carrier card or a similar computer I/O interface.

There are three I/O connectors on the GPSRF board. First is the antenna connector, J1. This connector is a female OSX or MCX RF connector. This RF connector has five volts on the center pin, which can be used with GPS antennas that contain a Low Noise Amplifier (LNA) or pre-amplifier for additional

signal gain. The second connector, JP4, is a 10-pin male, 2.54mm spacing connector, which is the primary 5-volt power connection for the GPSRF board. JP4 also contains discrete I/O connections to the GP2021 correlator IC (these lines are not currently being used but are there if needed in future releases – such as for timing applications). The third connector, JP5, is a 30 pin, 2.0 mm spacing male pin connector, which interfaces to the address/data/control lines of the GP2021 IC. Note that these are direct connection lines to the GP2021 and do not have ESD protection on them, so great care should be exercised when handling the GPSRF board to prevent damage to the correlator IC. See figure 2 for a block diagram of the GPS1005 GPS receiver board components.

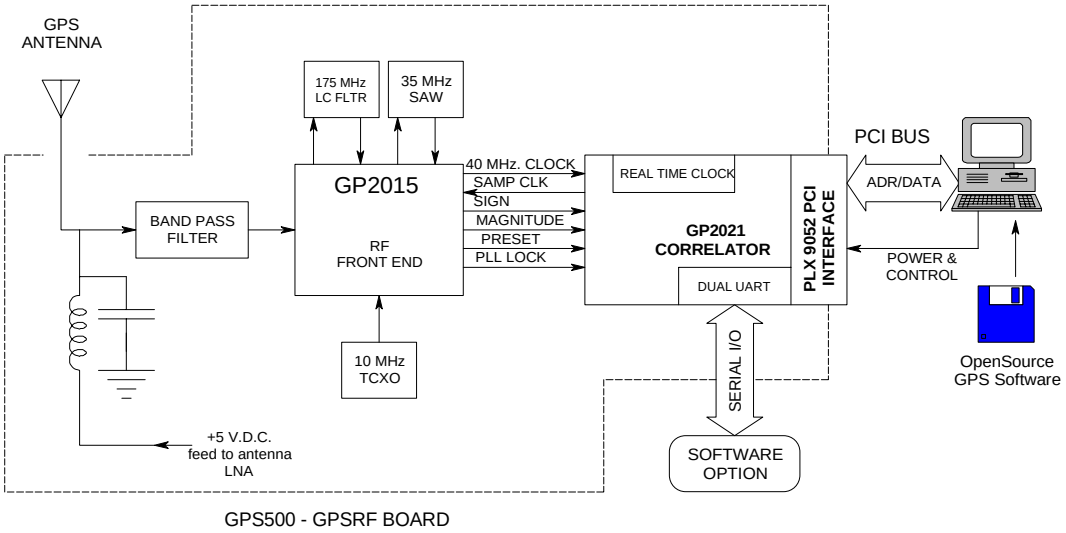

Figure 2. Block Diagram of GPSRF and GPS1005 Board

The GP2015 RF IC and the GP2021 correlator IC data sheets are included with the GPS1005 documentation and on the CD supplied with the board. Additional copies may be obtained from the Zarlink web site: http://products.zarlink.com/product_profiles/GP2021.htm . The GPSRF board contains the precision 10 MHz. oscillator for generating the frequencies needed by the GP2015 IC to mix with the GPS signals to convert the information down to lower frequencies where it is digitized and sent to the GP2021 correlator IC. The digitized signal leaving the GP2015 RFIC is at the frequency of 5.714 MHz. The correlator IC contains many functions including the C/A code generator, the Numerically Controlled Oscillator (NCO) and other circuitry necessary for decoding GPS signals. The 16 bit address and data lines from the correlator are brought out to the PCI bus card where the decoded data from the GPS satellites can be made available to the user running the GPS OpenSource software program on the PC.

For more information on OpenSource software, contact: Free software Foundation, Inc., 59 Temple Place, Suite 330, Boston, MA 02111-1307. The following statement is a quote from the Free Software Foundation's General Public License*: "When we speak of free software, we are referring to freedom, not price. Our General Public Licenses are designed to make sure that you have the freedom to distribute copies of free software (and charge for the service if you wish), that you receive source code or can get it if you want it, that you can change the software or use pieces of it in new free programs; and that you know you can do these things."* The GPS OpenSource software included in the GPS1005 kit is distributed in accordance with this license. For more information see: http://www.earthlink.net/~cwkelley

The GPS receiver OpenSource software is written in C++ language and can be compiled using a standard Borland C compiler (version 5.02). The Borland compiler is included in the GPS1005 kit. (NOTE: The compiler also is an optional item for those wanting to just experiment with compiling the OpenSource code – see the price list for details). The GPS receiver executable code is run under DOS. The PC and the DOS software are not included in the standard GPS1005 kit. However, for those customers that want to purchase a complete operational system, contact GPS Creations for a quote for the GPS1005 and a PCI bus-based computer including a DOS operating system.

Figure 3 shows the small GPSRF board. This board plugs into the PCI card carrier card and operates from the regulated 5 volt DC source supplied by the personal computer. The GPS1005 board has a SMA female RF connector for interface to the GPS antenna system (short coax cable to SMA bulkhead connector on the PC card metal plate. This connector has 5 volts on the center pin to feed the LNA used on most GPS antennas. **NOTE: Caution must be exercised to isolate the 5 volts if an antenna is used which does not have the 5 volt pre-amp or LNA circuit.** Many passive antennas have the center feed point grounded and if so, may short-circuit the 5 volts being fed by the GPSRF board. The antenna connector on the GPSRF board as standard is a MCX (also called OSX) connector. A "bias-tee" designed for GPS frequencies can be used to provide DC isolation and protect the GPS1005 board if a pre-amp antenna is not used. An application note on GPS antennas, installation and use is available from GPS Creations.

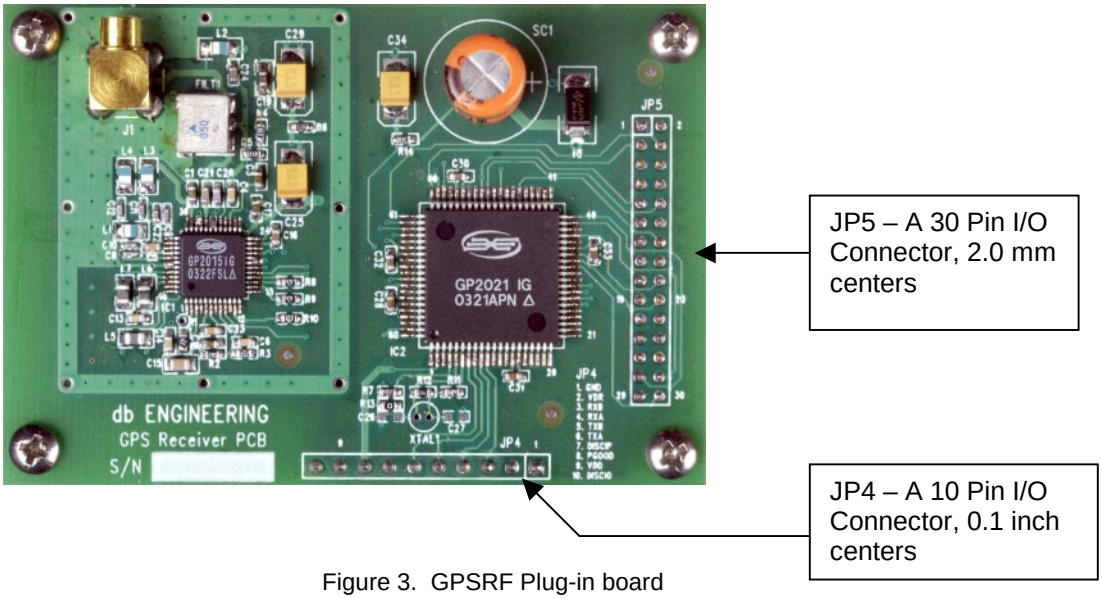

Figure 3. GPSRF Plug-in board

The GPSRF board is a four-layer PCB design with components located on both sides of the board. The component side has both GP2015 and GP2021 IC's and the underneath side contains the 10 MHz TCXO and 35 MHz IF SAW filter. The I/O connections of the GPSRF board are shown in tables 1 & 2.

Pin No.	Function	Pin No.	Function
1	Data Line 8	16	Data Line 6
2	Data Line 9	17	Data Line 7
3	Data Line 10	18	I/O Write
4	Data Line 11	19	I/O Enable
5	Data Line 12	20	I/O Read
6	Data Line 13	21	N/C
7	Data Line 14	22	Address Line 2
8	Data Line 15	23	Address Line 3
9	Data Line 4	24	Address Line 4
10	Data Line 3	25	Address Line 5
11	Data Line 2	26	Address Line 6
12	Data Line 1	27	Address Line 7
13	Data Line 0	28	Address Line 8
14	Address Latch Enable	29	Address Line 9
15	Data Line 5	30	Discrete I/O

Table 1. JP5, 30-pin Data/Address I/O connector – functions

The analog and digital sections of the GPSRF board each have their respective ground planes tied together at pin 1 of JP5. JP7 on the PCI board provides interface connections for the additional signals on JP5.

SECTION II – PCI CARD

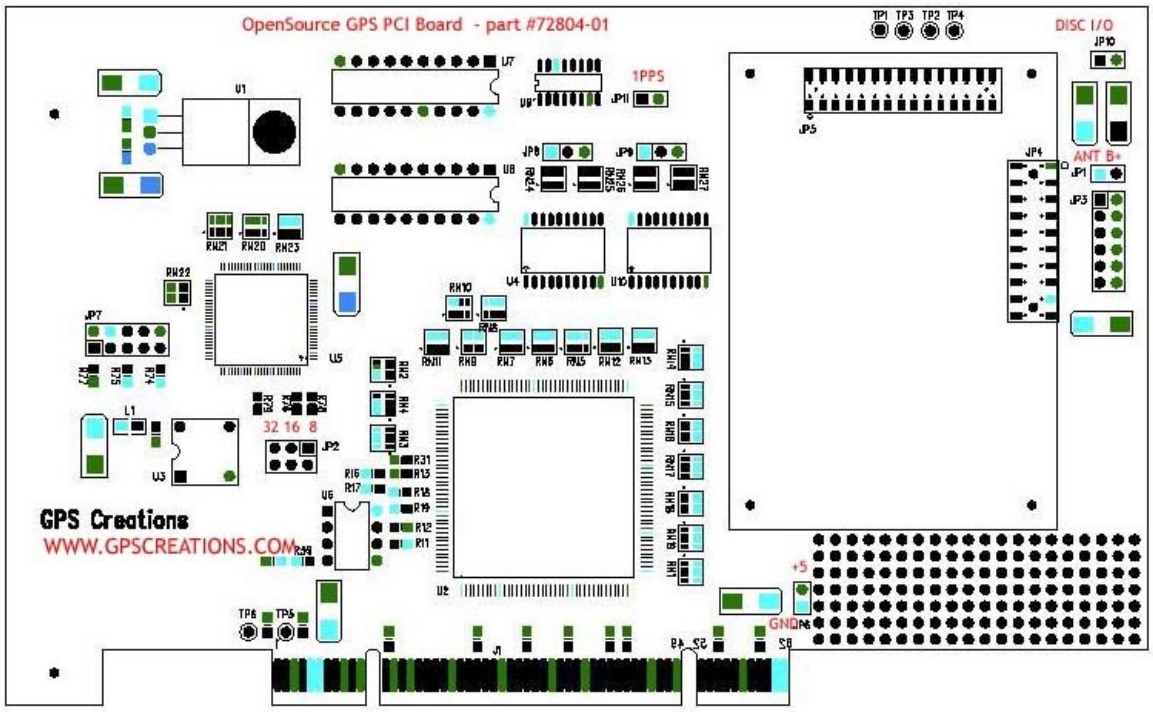

Figure 4. Parts view on GPS1005 PCI Board

Figure 5 shows the location of JP1. This jumper controls the "on board" feeding of 5 volts to the GPS Antenna (through the GPS500 RF board). To disable the 5-volt feed to the GPS antenna, remove JP1 as it is normally installed when shipped from the factory.

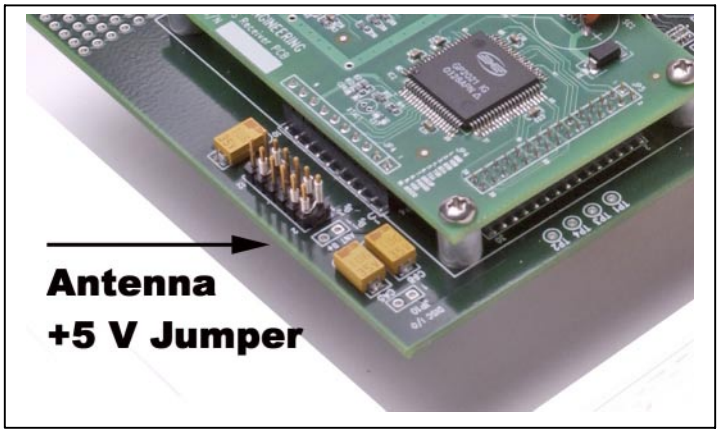

Figure 5. Five volt jumper for GPS antenna (JP1)

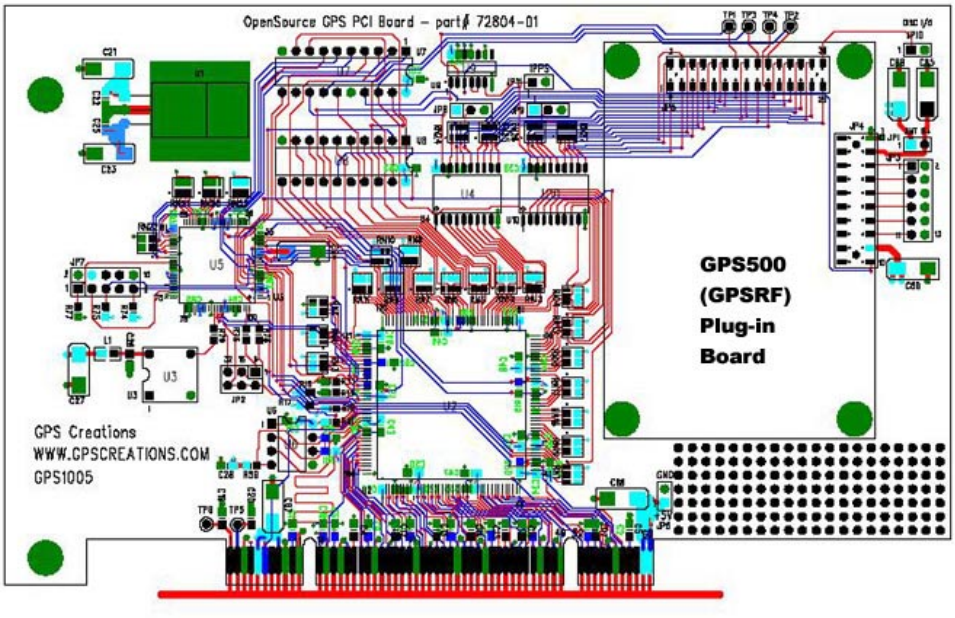

Figure 6. GPS1005 PCI Card Traces

The PCI board contains eight IC's. They consist of two each 74HCT245 bus interface chips, two each 16L8 PAL's for logic and address decoding, and a 74LS04 hex buffer. There are three devices providing interface to the PCI bus. Those are the PLX Technologies 9052 bridge IC, an Altera EPLD and a 93C46 EEPROM containing data about the PCI bus interface information. There are several unused

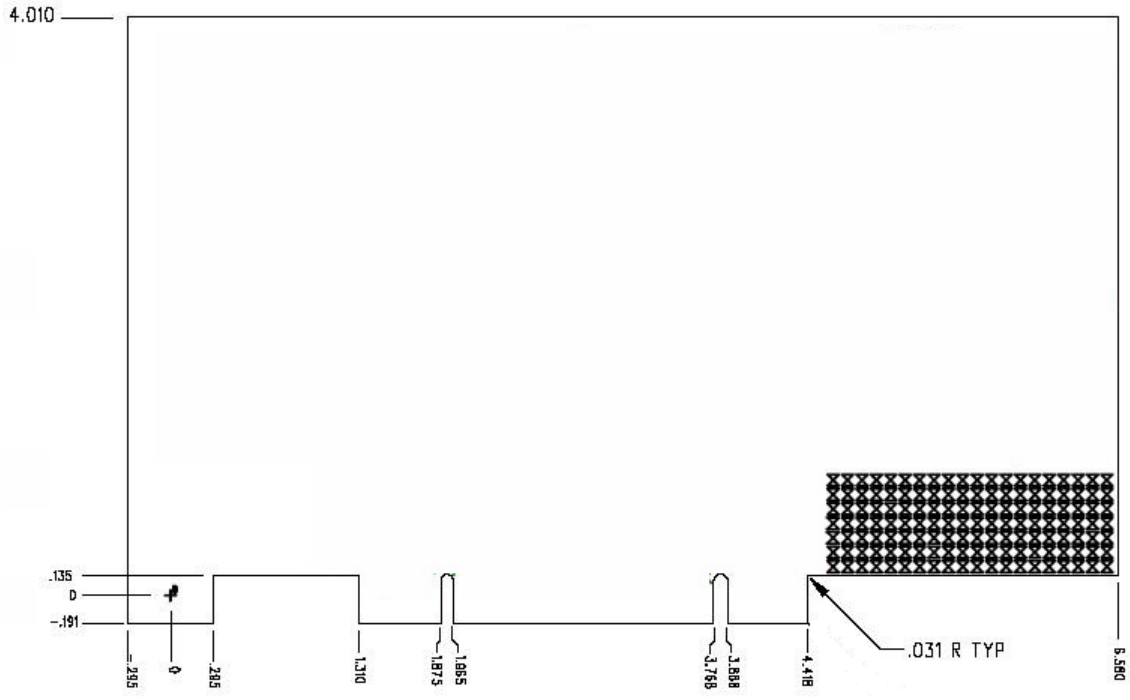

Figure 7. GPS1005 Mechanical Dimensions

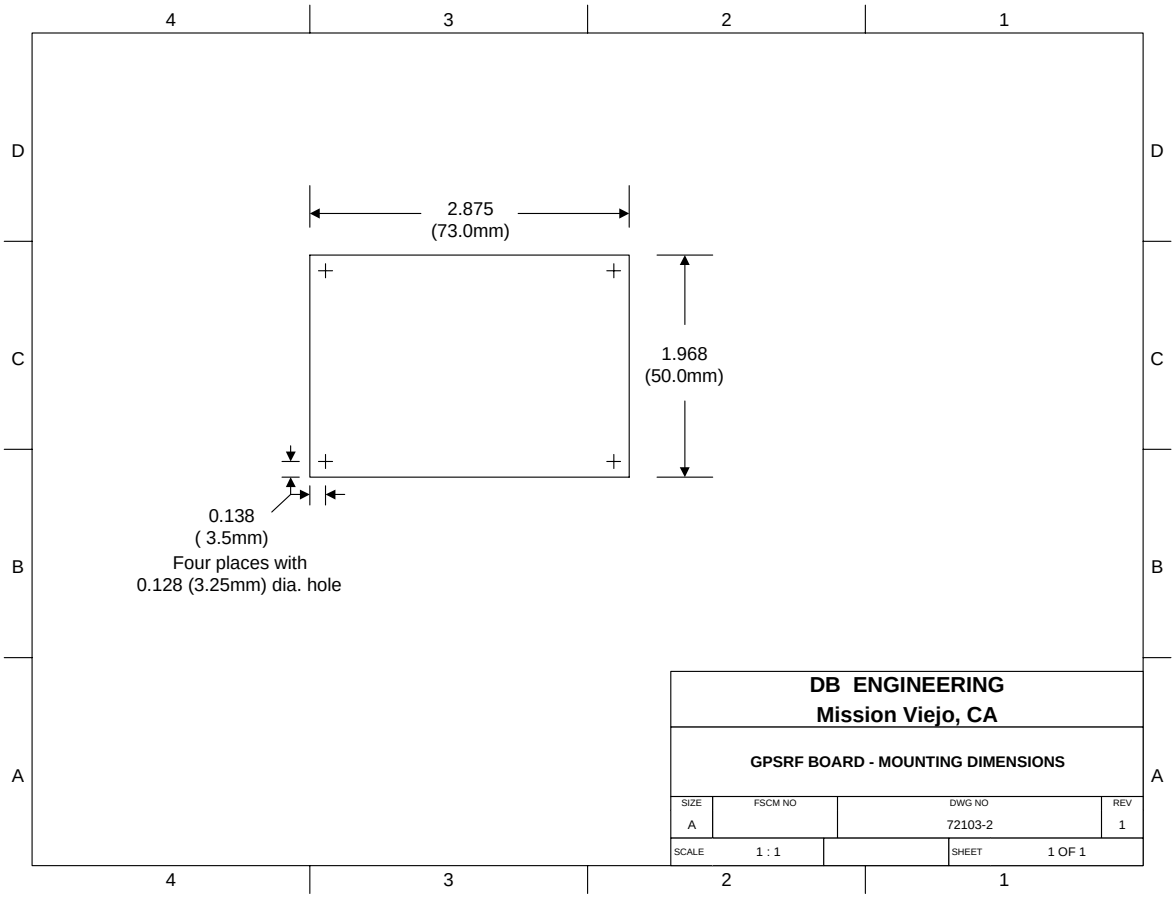

Figure 8. GPSRF Board Dimensions

functions on the GP2021 which are brought out to the PCI bus card for possible expansion uses. Also, there is a series of 0.1 inch spaced plated-thru holes for a prototyping area on the PCI board. Five volts and ground points are made available near the prototyping area.

Gold plating is provided on the PCI bus fingers for durability and minimal contact resistance. The GPS antenna coax connector is a SMA female installed on the PCI cards' metal end-bracket.

The schematics of both PCI bus card and the GPSRF board are provided in with the GPS1005 receiver kit. The schematics are in Orcad software and also provided in PDF format. There are 8.5 x11 paper copies provided in the reference manual as well. All construction information is provided to those purchasing the GPS1005 receiver kit. This design is intended in the spirit of OpenSource. However, reproduction of the hardware, drawings, schematics and documentation is not permissible without prior approval from GPS Creations.

GPS1005 Jumper Location Drawing

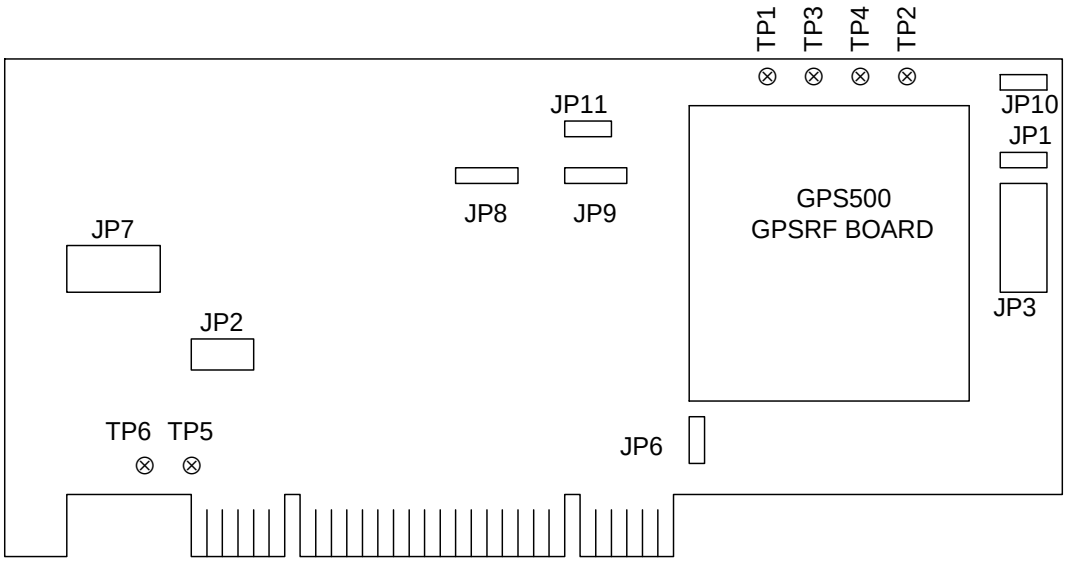

Figure 9. Jumper Configuration

ITEM	DESCRIPTION	FACTORY CONDITION
JP1	5 Volt feed to GPS Antenna LNA	Jumper Installed
JP2	8, 16, 32 MHz Select for PLX9052	8 MHz Selected
JP3-1	RXB (Input to GP2021)	Jumper Installed – Grounded
JP3-2	RXA (Input to GP2021)	Jumper Installed – Grounded
JP3-3	TXB (Output on GP2021)	Open
JP3-4	TXA (Output on GP2021)	Open
JP3-5	DISCIP – Discrete Input to GP2021	Jumper Installed – Grounded
JP3-6	PGOOD – Output on GP2021	Open
JP6	5 Volts for expansion area	No Connect
JP7	Altera EPLD Programming	No Connect
JP8	Pull-up, Pull-down Resistor Select	Jumper to Ground
JP9	Pull-up, Pull-down Resistor Select	Jumper to Ground
JP10	Discrete Input/Output pin on GP2021	No Connect
JP11	1PPS Output	No Connect

Table 4. GPS1005 Jumper Configuration

TP1 = Address Latch Enable
TP2 = Input/Output Read
TP3 = Input/Output Write
TP4 = GP2021Chip Select
TP5 = + 12 Volts D.C. (not used on the GPS1005)
TP6 = - 12 Volts D.C. (not used on the GPS1005)

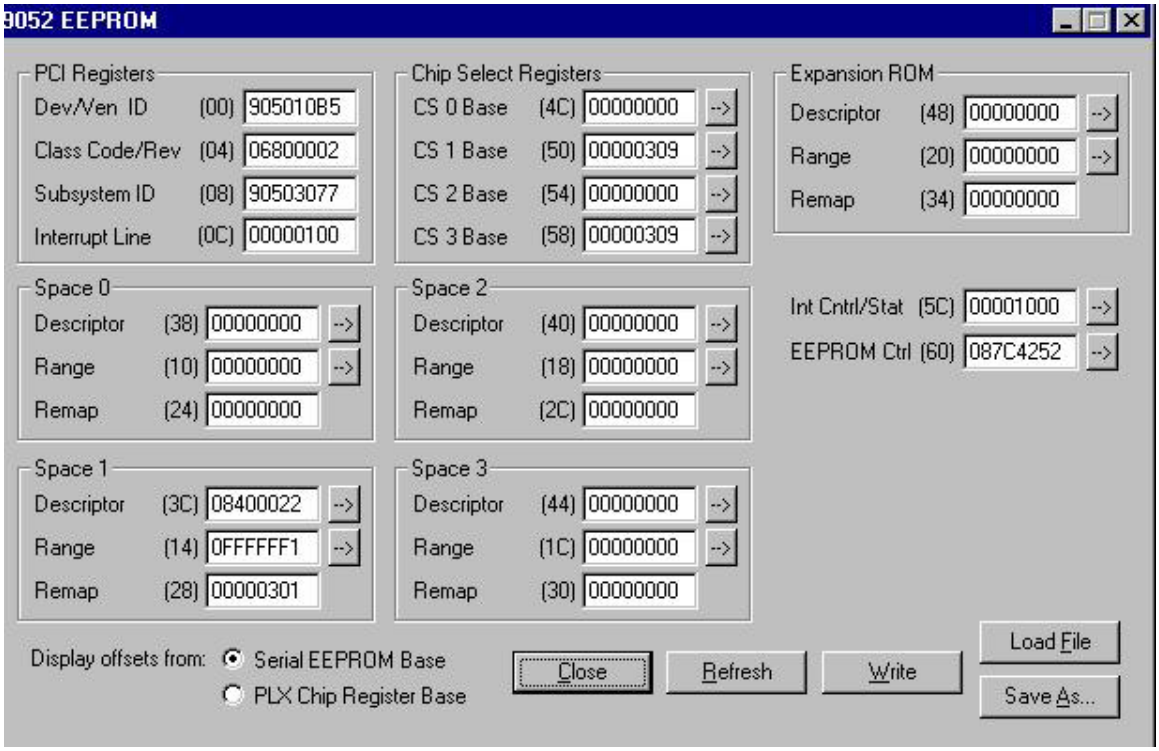

Figure 10. 93LC46 EEPROM contents.

United States International Trade in ARMS Regulation (ITAR) prevents sales of GPS receivers capable of providing navigation solutions at speeds in excess of 1,000 nautical miles/hour and altitudes in excess of 60,000 feet. This requirement limits some applications rendering many of the commercial GPS receivers useless. The GPS1005 receiver does conform to this requirement. The user is cautioned about removal of this limitation in the Opensource code. Included with the GPS1005 receiver is a copy of an application note on this restriction. Contact GPS Creations to request a PDF copy of the ITAR limitations document.

At the present time, the OpenSource GPS code (version 1.16) does not include WAAS satellite reception capability. However, the GP2021 correlator IC does. Future versions of the code may contain this functionality, or this may be a function the user desires to add. The GPS1005 hardware should support reception of the WAAS satellites (see the GP2021 data sheet for more information).

GPS Creations is not responsible for operation of the receiver if the user does not install the board correctly in the computer or properly install the software or operate the hardware in a manner in which it was intended. Also, correct operation of the receiver can only be obtained by having a properly designed GPS antenna installation. Information provided by GPS Creations is believed to be accurate and reliable. However, no responsibility is assumed by GPS Creations for its use, nor any infringement of patents, or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent rights of GPS Creations other than for circuitry embodied in GPS Creations products. GPS Creations reserves the right to change circuitry at any time without notice. This document is subject to change without notice.